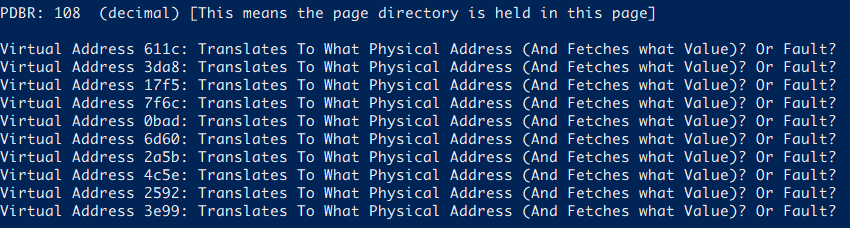
**Homework Wan Huzaifah bin Wan Azhar**

**Answer:**

For multi-page table, the system still only needs one register. As the process has its own page table, the address of the page table is stored into the process’s process control block. When the process attempts to access its memory, it will simply get the master page table address and then index into the page table into the next level and so on until it gets the correct address. It is noted that the cost of TLB miss is huge.

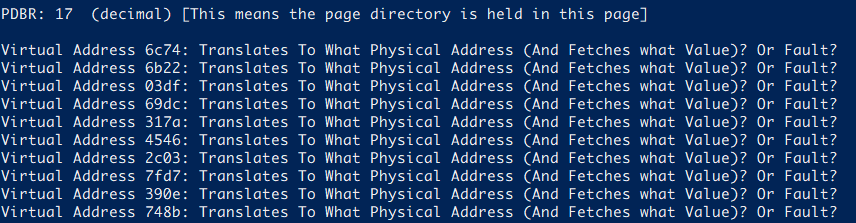
1. The exercise asks me to do 3 Seed of 10 Address. But I will only do 2 Seed of 5 Address.

Seed 0



1. Virtual Address 611c
   1. 611c to binary: 11000 01000 11100
   2. First PDE: 0xA1
   3. 0xA1 to binary: 10100001
   4. 1 (valid bit) 0100001 (Page 33)
   5. Second PTE (from a.): 01000 to decimal: 8
   6. PTE: 0xB5 to binary: 10110101
   7. 1 (valid bit) 0110101 (Page 53)
   8. Third offset (from a.): 11100 to decimal 28
   9. 0110101 (from g) 11100 (from h) -> Hex = 0x6BC Physical address of memory
   10. Value: 08
2. Virtual Address 3DA8
   1. 3DA8 to binary: 01111 01101 01000
   2. First PDE: 0xD6
   3. 0xD6 to binary: 11010110
   4. 1 (valid bit) 1010110 (Page 86)
   5. Second PTE (from a.): 01101 to decimal: 13
   6. PTE: 0x7F to binary: 01111111
   7. 0 (Invalid bit) 1111111 (Page 127)
   8. Fault (invalid bit)
3. Virtual Address 17F5
   1. 17F5 to binary: 00101 11111 10101
   2. First PDE: 0xD4
   3. 0xA1 to binary: 11010100
   4. 1 (valid bit) 1010100 (Page 84)
   5. Second PTE (from a.): 11111 to decimal: 31
   6. PTE: 0xCE to binary: 11001110
   7. 1 (Valid bit) 1001110 (Page 78)
   8. Third offset (from a.): 10101 to decimal 21
   9. 1001110 (from g) 10101 (from h) -> Hex = 0x9D5 Physical address of memory
   10. Value: 1C
4. Virtual Address 7F6C
   1. 7F6C to binary: 11111 (31) 11011 01100
   2. First PDE: 0xFF
   3. 0xFF to binary: 11111111
   4. 1 (valid bit) 1111111 (Page 127)
   5. Second PTE (from a.): 11011 to decimal: 27
   6. PTE: 0x7F to binary: 01111111
   7. 0 (Invalid bit) 1111111 (Page 127)
   8. Fault (invalid bit)
5. Virtual Address 0BAD
   1. 0BAD to binary: 00010 (2) 11101 01101
   2. First PDE: 0xE0
   3. 0xE0 to binary: 11100000
   4. 1 (valid bit) 1100000 (Page 96)
   5. Second PTE (from a.): 11101 to decimal: 29
   6. PTE: 0x7F to binary: 01111111
   7. 0 (Invalid bit) 1111111 (Page 127)
   8. Fault (invalid bit)

Seed 1



1. Virtual Address 6C74
   1. 6C74 to binary: 11011 (27) 00011 10100
   2. First PDE: 0xA0
   3. 0xA0 to binary: 1 0100000
   4. 1 (valid bit) 0100000 (Page 32)
   5. Second PTE (from a.): 00011 to decimal: 3
   6. PTE: 0xE1 to binary: 11100001
   7. 1 (Valid bit) 1100001 (Page 97)
   8. Third offset (from a.): 10100 to decimal 20
   9. 1100001 (from g) 10100 (from h) -> Hex = 0xC34 Physical address of memory
   10. Value: 06
2. Virtual Address 6B22
   1. 6B22 to binary: 11010 (26) 11001 00010
   2. First PDE: 0xD2
   3. 0xD2 to binary: 11010010
   4. 1 (valid bit) 1010010 (Page 82)
   5. Second PTE (from a.): 11001 to decimal: 25
   6. PTE: 0xC7 to binary: 11000111
   7. 1 (Valid bit) 1000111 (Page 71)
   8. Third offset (from a.): 00010 to decimal 2
   9. 1000111 (from g) 00010 (from h) -> Hex = 0x8E2 Physical address of memory
   10. Value: 1A
3. Virtual Address 03DF
   1. 03DF to binary: 00000 11110 11111
   2. First PDE: 0xDA
   3. 0xDA to binary: 11011010
   4. 1 (valid bit) 1011010 (Page 90)
   5. Second PTE (from a.): 11110 to decimal: 30
   6. PTE: 0x85 to binary: 10000101
   7. 1 (Valid bit) 0000101 (Page 5)
   8. Third offset (from a.): 11111 to decimal 31
   9. 0000101 (from g) 11111 (from h) -> Hex = 0x0BF Physical address of memory
   10. Value: 0F
4. Virtual Address 69DC
   1. 69DC to binary: 11010 (26) 01110 11100
   2. First PDE: 0xD2
   3. 0xD2 to binary: 11010010
   4. 1 (valid bit) 1010010 (Page 82)
   5. Second PTE (from a.): 01110 to decimal: 14
   6. PTE: 0x7F to binary: 01111111
   7. 0 (Invalid bit) 1111111 (Page 127)
   8. Fault (invalid bit)
5. Virtual Address 317A
   1. 317A to binary: 01100 (12) 01011 11010
   2. First PDE: 0x98
   3. 0xDA to binary: 10011000
   4. 1 (valid bit) 0011000 (Page 24)
   5. Second PTE (from a.): 01011 to decimal: 11
   6. PTE: 0xB5 to binary: 10110101
   7. 1 (Valid bit) 0110101 (Page 53)
   8. Third offset (from a.): 11010 to decimal 26
   9. 0010101 (from g) 11010 (from h) -> Hex = 0x6BA Physical address of memory
   10. Value: 1E
6. It will leads to lots of cache miss.
   1. This is because due to spatial locality and temporal locality, which states that if a process access a part of data in a location, the next access will most likely in the closest part in the location.
   2. As such, because page table does not organize itself into group like stacks, data, etc. It will not leads to such locality and such more miss.